

Amendment to the Claims:

The following listing of claims will replace all prior listings in this application.

Listing of claims:

1. (Currently amended) A semiconductor component comprising:
a semiconductor substrate having an insulating layer on the semiconductor substrate surface and having a capacitance structure in the insulating layer, wherein the capacitance structure comprises:
a first substructure which has a first cohesive latticed metal region including crossing metal leads which extends in a first common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the first cohesive latticed metal region in each of its subregions from above and from below,
wherein the first cohesive latticed metal region is electrically connected to a first connecting line; and
~~a first substructure having~~ electrically conductive regions arranged in ~~cutouts openings~~ in the first cohesive latticed metal region of the first substructure at a distance from edge regions of the ~~cutouts openings~~ in the common plane,
wherein the electrically conductive regions are electrically connected to a second connecting line, and
wherein the electrically conductive regions comprise one of metal plates or node points between via connections.
2. (Currently amended) The semiconductor component as claimed in claim 1, wherein the capacitance structure further comprises:
a second substructure parallel to and at a distance from the first substructure wherein the second substructure comprises:
a second cohesive latticed metal region including crossing metal leads which extends in a second common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region in each of its subregions from above and below; and

electrically conductive regions, and
wherein the first and second substructures are electrically connected by
the first and second connecting lines.

3. (Currently amended) The semiconductor component as claimed in claim 2, wherein the second substructure is of substantially the same design as the first substructure, and the first and second substructures are arranged laterally offset from one another such that the electrically conductive regions of the first substructure are arranged vertically above crossing points of the metal leads in the second cohesive latticed metal region of the second substructure, and crossing points of the metal leads in the first cohesive latticed metal region of the first substructure are arranged vertically above the electrically conductive regions of the second substructure.

4. (Currently amended) The semiconductor component as claimed in claim 3, wherein the crossing points of the metal leads in the first cohesive latticed metal region of the first substructure are electrically connected to the electrically conductive regions of the second substructure and the electrically conductive regions of the first substructure are electrically connected to the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure, by means of at least one respective via connection.

5. (Currently amended) The semiconductor component as claimed in claim 2, wherein the second cohesive latticed metal region of the second substructure is laterally offset from the first substructure, so that the electrically conductive regions of the first substructure are arranged vertically above the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure.

6. (Currently amended) The semiconductor component as claimed in claim 5, wherein the electrically conductive regions of the first substructure and the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure are electrically connected by means of one or more respective via connections.

7. (Currently amended) The semiconductor component as claimed in claim 2 claim 3 further comprising a metal plate electrically connected to one of the crossing points of the metal leads in a the cohesive latticed metal region of the first and second substructure or and to the electrically conductive regions of the first and second substructures substructure by means of one of or more respective via connections.

8. (Currently amended) The semiconductor component as claimed in claim 1, wherein the first cohesive latticed metal region has at least two square or round cutouts openings.

9. (New) The semiconductor component as claimed in claim 1, wherein the first and second connecting lines are at different electrical potentials.

10. (New) The semiconductor component as claimed in claim 1, wherein a first non-parasitic capacitance exists between the cohesive latticed metal region of the first substructure and a second non-parasitic capacitance exists between the first and second connecting lines, and wherein the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance.

11. (New) A semiconductor component having an integrated capacitance structure, the component comprising:

a semiconductor substrate having a surface;
an insulating layer overlying the surface of the semiconductor substrate;
a capacitance structure in the insulating layer, wherein the capacitance structure comprises:

a first metal lattice including intersecting metal leads in a first common plane parallel to the substrate surface;

a second metal lattice including intersecting metal leads in a second common plane parallel to the substrate surface,

electrically conductive regions arranged in openings in the first and second metal lattices, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice are substantially vertically above crossing points of the second metal lattice, and crossing points of the first metal lattice are substantially vertically above the electrically conductive regions of the second metal lattice; and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential.

12. (New) The semiconductor component as claimed in claim 11, wherein the electrically conductive regions comprise metal plates or node points.

13. (New) The semiconductor component as claimed in claim 11, wherein the electrical connections comprise:

first connecting lines electrically connecting the electrically conductive regions of the first metal lattice to crossing points of the second metal lattice; and

second connecting lines electrically connecting crossing points of the first metal lattice to the electrically conductive regions of the second metal lattice.

14. (New) The semiconductor component as claimed in claim 11 further comprising a metal plate in a third common plane parallel to the substrate surface and electrically coupled to the first and second metal lattices by the first and second electrical connections.

15. (New) The semiconductor component as claimed in claim 11 further comprising a third metal lattice including intersecting metal leads in a third common plane parallel to the substrate surface, wherein the intersecting metal leads define openings, wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections.

Claim 3 recites additional features of the semiconductor component of Claim 2, in which the first and second substructures are laterally offset from one another. The lateral offset arrangement results in the separate regions of each substructure being alternately aligned. The vertical alignment is such that the crossing points of one substructure are vertically aligned with the electrically conductive regions of the other substructure, and vice versa. The Applicant asserts that such an alignment relationship is not suggested or disclosed by Kuroda et al., at least because the various overlying electrodes all have similar geometric features.

Claim 5 depends from Claim 3 and recites that the different regions of the first and second substructures are electrically connected by means of respective via connections.

Claim 5 depends from Claim 2 and recites the lateral offset relationship of the first and second substructures.

Claim 6 recites that the crossing points of the first substructure are electrically connected to the electrically conductive regions of the first substructure by one or more respective via connections.

Claim 7 depends from Claim 3 and recites that a metal plate is electrically connected to the crossing points of the metal leads in the cohesive lattice metal region of the first substructure, and to the electrically conductive regions of the second substructure by means of one or more respective via connections.

Claim 8 recites that the first cohesive lattice metal region has at least two square or round openings.

New Claims

Claims 9-21 are newly added to the application in order that the Applicant may more fully claim the subject matter of their invention.

Claim 9 depends from Claim 1 and recites that the first and second connecting lines are at different electrical potentials.

Claim 10 depends from Claim 1 and recites that first and second non-parasitic capacitances exist in the semiconductor component. These capacitances arise

16. (New) A semiconductor component having an integrated capacitance structure, the capacitance structure comprising:

an insulating layer;

a first metal lattice in the insulating layer, the first metal lattice including intersecting metal leads in a first common plane;

a second metal lattice in the insulating layer, the second metal lattice including intersecting metal leads in a second common plane,

electrically conductive regions arranged in openings in at least one of the first and second metal lattices, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice are substantially vertically above crossing points of the second metal lattice, and crossing points of the first metal lattice are substantially vertically above the electrically conductive regions of the second metal lattice;

a third metal structure in the insulating layer in a third common plane the third metal structure comprising one of a third metal lattice or a metal plate; and

first and second electrical connections between the first and second lattices and the third metal structure, such that the first and second electrical connections are at different electrical potential.

17. (New) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a metal plate electrically coupled to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

18. (New) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a third metal lattice including intersecting metal leads, wherein the intersecting metal leads define openings, wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

19. (New) The semiconductor component as claimed in claim 16, wherein the first electrical connection electrically connect the electrically conductive regions of the first metal lattice to the crossing points of the second metal lattice, and wherein the second electrical connection electrically connect the crossing points of the first metal lattice to the electrically conductive regions of the second metal lattice.

20. (New) The semiconductor component as claimed in claim 16, wherein the third metal structure comprises a third metal lattice including intersecting metal leads and electrically conductive regions in openings defined by the intersecting metal leads.

21. (New) The semiconductor component as claimed in claim 20, wherein non-parasitic capacitances exist between the electrically conductive regions and intersecting metal leads in the first, second, and third metal lattices and wherein non-parasitic capacitances exist between the first and second connecting lines.